WHAT IS CLAIMED IS:

1. An interface circuit, comprising:

a first port for providing an IDE interface with a host computer;

a second port for providing an IDE interface with a data storage device; and

a control circuit, operatively coupled between the first and second ports, that sends an invalid command rather than a selected IDE command to the second port in response to receiving the selected IDE command at the first port.

2. The interface circuit of claim 1, wherein the selected IDE command is from the group consisting of a write, media lock, media unlock, sleep, standby, download microcode and packet command.

3. The interface circuit of claim 1, wherein the selected IDE command is a write command.

4. The interface circuit of claim 1, wherein the control circuit sends the invalid command to the second port in response to any of a plurality of selected IDE commands received at the first port and prevents the second port from receiving any of the selected IDE commands.

5. The interface circuit of claim 4, wherein two of the selected IDE commands are from the group consisting of a write, media lock, media unlock, sleep, standby, download microcode and packet command.

6. The interface circuit of claim 4, wherein one the selected IDE commands is a write command.

7. The interface circuit of claim 1, wherein the invalid command is a reserved IDE command.

8. The interface circuit of claim 7, wherein the reserved IDE command is 01h.

9. The interface circuit of claim 1, wherein the control circuit sends a read command received at the first port to the second port.

10. The interface circuit of claim 1, wherein the control circuit sends each of a plurality of IDE commands received at the first port to the second port, wherein the plurality of IDE commands includes a read command and excludes a write command.

11. The interface circuit of claim 1, wherein the control circuit sends any IDE command other than a write command received at the first port to the second port.

12. The interface circuit of claim 1, wherein the control circuit sends any IDE communication received at the second port to the first port.

13. The interface circuit of claim 1, wherein the selected IDE command is a write command, the invalid command is a reserved IDE command, the control circuit sends each of a plurality of IDE commands that includes a read command and excludes the write command and is received at the first port to the second port, and the control circuit sends any IDE communication received at the second port to the first port.

14. The interface circuit of claim 1, including an external device that permits a user to enable and disable a command-inhibit function of the control circuit, wherein when the command-inhibit function is enabled then the control circuit sends the invalid command rather than the selected IDE command to the second port in response to the selected IDE command being received at the first port, and when the command-inhibit function is disabled then the control circuit sends the selected IDE command rather than the invalid command to the second port in response to the selected IDE command being received at the first port.

15. The interface circuit of claim 14, wherein the external device is a mechanical switch that the user can toggle to enable and disable the command-inhibit function.

16. The interface circuit of claim 14, wherein the external device is a pair of jumper pins for which the user can insert and remove a jumper to enable and disable the command-inhibit function.

17. The interface circuit of claim 1, wherein the control circuit includes a logic device and a data switch, the logic device is coupled to the lower eight data bus bits and the three address bits and the I/O write signal of the first port, the data switch is coupled to the lower eight data bus bits of the first and second ports and to the logic device, and the data switch selectively couples the lower eight data bus bits of the second port to one of the lower eight data bus bits of the first port and the invalid command in response to the logic device.

18. The interface circuit of claim 1, wherein the first port is a 40-pin male IDE connector and the second port is a 40-pin female IDE connector.

19. The interface circuit of claim 1, including a printed circuit board, wherein the first and second ports and the control circuit are mounted on the printed circuit board, and the first and second ports extend from opposing major surfaces of the printed circuit board.

20. The interface circuit of claim 1, in combination with an IDE hard disk drive connected to the second port.

21. A computer system, comprising:

a host computer;

a hard disk drive; and

an interface circuit coupled between an IDE port of the host computer and an IDE port of the hard disk drive, wherein the interface circuit provides an IDE communication link between the host computer and the hard disk drive, the interface circuit sends a read command received by the host computer to the hard disk drive, thereby allowing the host computer to read from the hard disk drive, and the interface circuit sends an invalid command to the hard disk drive in response receiving a write command from the host computer, thereby preventing the host computer from writing to the hard disk drive.

22. The computer system of claim 21, wherein the interface circuit includes a first 40-pin connector coupled to the IDE port of the host computer, a second 40-pin connector coupled to the IDE port of the IDE hard disk drive, a third 4-line connector coupled to a power supply port of the host computer, and a fourth 4-line connector coupled to a power supply port of the hard disk drive.

23. The computer system of claim 22, wherein the first 40-pin connector is connected to an IDE ribbon cable, the IDE ribbon cable is connected to the IDE port of the host computer, and the second 40-pin connector is connected to the IDE port of the hard disk drive.

24. The computer system of claim 21, wherein the interface circuit sends any command received from the host computer other than a write command to the hard disk drive, thereby allowing the host computer to instruct the hard disk drive to perform non-write operations.

25. The computer system of claim 24, wherein the interface circuit sends any communication received from the hard disk drive to the host computer, thereby allowing the hard disk drive to access the host computer.

26. The computer system of claim 21, wherein the hard disk drive generates an error message in response to the invalid command, and the interface circuit allows the host computer to read the error message, thereby informing the host computer that the write operation has failed.

27. The computer system of claim 21, wherein the interface circuit includes an external device that permits a user to enable and disable a write-inhibit function of the control circuit, wherein when the command-inhibit function is enabled then the control circuit sends the invalid command rather than the write command to the hard disk drive in response to the write command being received from the host computer, thereby preventing the host computer from writing to the hard disk drive, and when the command-inhibit function is disabled then the control circuit sends the write command rather than the invalid command to the hard disk drive in response to the write command being received from the host computer, thereby allowing the host computer to write to the hard disk drive.

28. The computer system of claim 21, wherein the control circuit defines a first set of IDE commands that includes the read command and a second set of IDE commands that includes the write command, the control circuit sends each of the first set of IDE commands received by the host computer to the hard disk drive, thereby allowing the host computer to implement the first set of IDE commands, and the control circuit sends the invalid command rather than any of the second set of IDE commands received by the host computer to the hard disk drive, thereby preventing the host computer from implementing the second set of IDE commands.

29. The computer system of claim 21, wherein the invalid command is a reserved IDE command.

30. The computer system of claim 21, wherein the computer system is a gaming machine.

31. A method of informing a host computer that an attempted operation on a data storage device has been prevented, comprising:

sending a IDE command from the host computer to a first IDE bus not connected to the data storage device;

determining that the data storage device should not receive the IDE command;

sending an invalid command rather than the IDE command to a second IDE bus connected to the data storage device; and

sending an error message generated by the data storage device in response to the invalid command from the data storage device to the host computer via the first and second IDE buses.

32. The method of claim 31, wherein the IDE command is a write command.

33. The method of claim 31, wherein the host computer periodically sends another IDE command to the data storage device via the first and second buses to determine whether the data

storage device received the IDE command that should not have been received by the data storage device.

34. The method of claim 31, wherein the first IDE bus includes a ribbon cable and the second IDE bus excludes a ribbon cable.

35. The method of claim 31, wherein the data storage device is a hard disk drive.

36. A method of preventing a host computer from writing to a data storage device, comprising:

sending a write command from the host computer to a first IDE bus not connected to the data storage device; and

sending an invalid command rather than the write command to a second IDE bus connected to the data storage device such that when the host computer deasserts an IDE I/O write signal the data storage device recognizes the invalid command rather than the write command, thereby preventing the host computer from writing to the data storage device.

37. The method of claim 36, further comprising sending an error message that the data storage device generates in response to the invalid command from the data storage device to the host computer via the first and second IDE buses.

38. The method of claim 36, further comprising sending a read command from the host computer to the data storage device via the first and second IDE buses to determine whether the write command was recognized by the data storage device.

39. The method of claim 36, wherein first IDE bus includes a ribbon cable and the second IDE bus excludes a ribbon cable.

40. The method of claim 36, wherein the data storage device is a hard disk drive.